Ka-BAND MONOLITHIC GaAs TWO-STAGE POWER AMPLIFIER

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ABSTRACT

A Ka-band monolithic GaAs two-stage power amplifier with 3.6 mm total gate width has been developed. It has delivered an output power at 1dB gain compression point of 0.56 W with 7.2 dB gain and 15 % power-added efficiency at 28 GHz. The performance obtained may be the highest power/gain yet reported on Ka-band monolithic GaAs amplifiers.

INTRODUCTION

Recent progress in fabrication technology and design technique has made it possible to develop monolithic GaAs power amplifiers at Ka-band[1,2].

The amplifiers reported so far are of single-stage and employ relatively small gate width FETs. Accordingly, the output power and gain are not sufficient enough for practical use.

The purpose of this paper is to report on two-stage monolithic power amplifier with larger gate width devices. The developed monolithic amplifier uses 1.2 mm and 2.4 mm gate width FETs for the 1st- and the 2nd-stage devices, respectively. The amplifier delivers an output power of 0.56 W, with a power gain of 7.2 dB, and a power-added efficiency of 15 % at 28 GHz. Output power more than 0.5 W is obtained over 27.5-28.5 GHz with power gain exceeding 5 dB. To the authers' knowledge, the results presented here are the best performance reported so far on a Ka-band single chip amplifiers.

DEVICE STRUCTURE

The basic FET structure used in this amplifier is similar to that used in the previously reported pseudo MMIC providing 1 W of output power and 4.2 dB of power gain at 29.5 GHz[3]. Fig.1 shows a SEM photograph of the second-stage FET part in the developed monolithic amplifier. The source overlay structure is adopted in order to reduce FET lateral dimensions, and at the same time to obtain a very low source inductance. The gate fingers are combined by a gate bus bar, and the source fingers are connected by air bridges across the gate bus bar to the source pads. These source pads are grounded through via holes to the PHS formed on the back side of the substrate. Narrow recess structure is adopted to reduce the effect of the surface depletion layer. The nominal gate length is 0.6 μm. The gate to gate spacing is 14 μm.

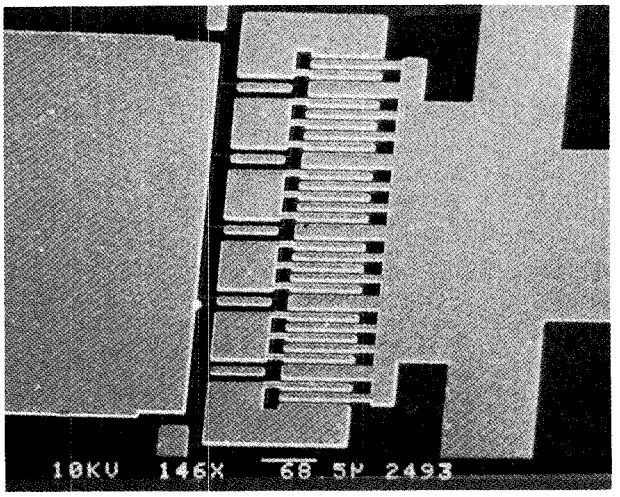

Fig.1. Photograph of second-stage FET part of two-stage amplifier

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AMPLIFIER DESIGN

The cluster matching approach is commonly used in monolithic power amplifier design. This technique has an advantage that impedance of smaller FETs are higher than aggregate FET and is therefore easier to match. However, it has a disadvantage that it requires a large area of matching circuit, resulting in a large chip size. In this study, we adopted an aggregate matching approach in order to obtain high power from a smaller chip.

An equivalent circuit of the developed two-stage power amplifier is shown in Fig.2. The input matching circuit uses open circuited stubs (L1, L2) and a quarter-wave length transformer. The output circuits uses short circuited stubs (L4, L5) and a quarter-wave length transformer. The gate widths of the first- and the second-stage FETs are 1.2mm and 2.4mm, respectively. Unit finger lengths are 50 μm and 80 μm for the first and the second-stage FETs. The difference of unit finger lengths makes it easier to design the interstage matching circuitry. Fig.3 shows the impedances of the output port of the first-stage FET and the input port of the second-stage FET. The input port impedance of the second-stage FET (Zin) is transformed to (Zin') by a uniform transmission line (L3), which is equal to the optimum power output port impedance of the first-stage FET (Z^*_{out}). The line width (W) and length (L) of this transmission line (L3) are determined by the following equations.

$$Z^*_{out} = Z_{L3}\frac{Z_{in} + jZ_{L3}\tan\beta L}{Z_{L3} + jZ_{in}\tan\beta L}$$

$$Z_{L3} = \frac{120}{\sqrt{\kappa_{eff}}}\left[\frac{W}{H} + 1.393 + 0.667\ln\left(\frac{W}{H} + 1.444\right)\right]^{-1}$$

where

β propagation constant,
H thicness of substrate,
Z_{L3} characteristic impedance of L3,
κ_{eff} effective dielectric constant

The calculated line width (W) is almost the same as the lateral dimension of the first and the second-stage FETs, resulting in uniform phase and amplitude operation of FETs.

Fig.4 shows the top view of the developed monolithic amplifier. The chip size is 3.4 x 1.9 x 0.08mm.

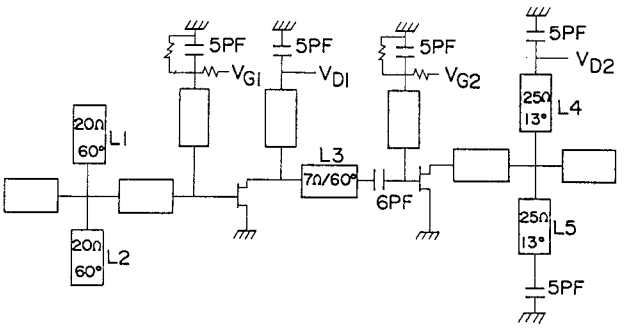

Fig.2. Schematic showing circuit element of two-stage amplifier

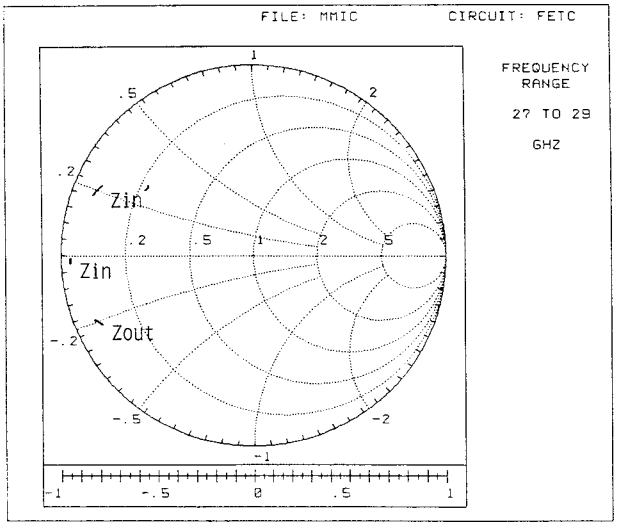

Fig.3. Impedances of FETs used for interstage circuit design

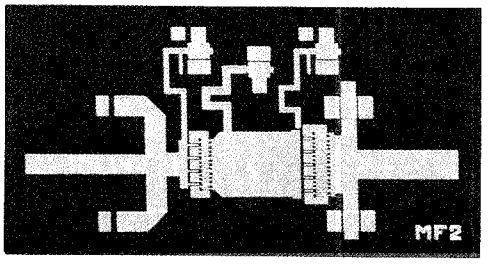

Fig.4. Picture of two-stage power amplifier

FABRICATION

The undoped LEC semi-insulating GaAs wafers are selectively implanted with Si+ and Be+ ions to form active channel layers. First, Si+ ions have been implanted at $4x10^{12}$ cm^{-2} and 50 keV plus $1.5x10^{13}$ cm^{-2} and 130keV and then Be+ ions have been implanted at $1.8x10^{12}$ cm^{-2} and 130keV. N+ contact layers are formed by Si implantation. Implanted wafers are capless annealed at 850 °C for 15min. in pure Ar ambient containing a small amount of AsH3. The peak carrier concentration of the channel layer is $4x10^{17}$ cm^{-3}. After the source and drain metalization are completed, gate and MIM capacitor base metal are defined by lifting off Al. The channel is passivated with PECVD Si_3N_4 which also serves as the dielectric layer of the MIM capacitors in the circuitry. The top metalization is Ti/Pt/Au of 4 μm thickness. After the front side processing are completed, substrates are thinned down to 40 ± 5 μm thickness, and via holes for grounding sources and shunting capacitors are formed by RIE using compound gases of BCl_3 and Cl_2. 40 μm thick plated gold heat sink interconnects all the via holes. Chip isolation is also performed by RIE.

MEASURED PERFORMANCE

Typical I-V characteristics of a 600 μm gate width monitor FET is shown in Fig.5. The saturation drain current, transconductance and pinch-off voltage are 130 mA (220 mA/mm),120 mS (200 mS/mm) and 1.5 V, respectively. The gate to drain breakdown voltage is ~8 V defined at 10 μA/mm leak current level. Monolithic amplifiers are DC screened and assembled on a W-Cu carrier with alumina substrates. Assembled monolithic amplifier is shown in Fig.6.

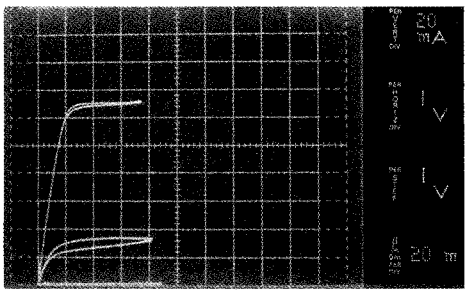

Fig.5. Tyipical I-V characteristics of monitor FET (Wg=600μm)

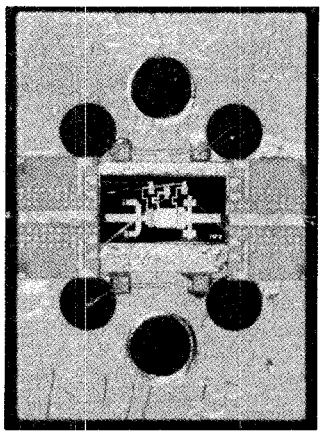

Fig.6. Assembled two-stage amplifier

Measured frequency response of the developed two-stage amplifier is shown in Fig.7. The bias conditions for the first- and the second-stage FETs are the same (Vg=-0.5V, Vds=6.5V) Small-signal gain over 5 dB has been obtained from 27 to 29 GHz, peaking to 8.2 dB at 28.0 GHz. Output power over 0.5 W with high gain has been obtained from 27.5 to 28.5 GHz. Fig.8 shows input-output characteristics and power-added efficiency measured at 28 GHz. At 1 dB gain comprresion point, the amplifier delivers an output power of 0.56 W (27.5 dBm) with 15 % of power-added efficiency. The figure of this power-added efficiency corresponds to 22 % for each FETs. A maximum output power of 0.76 W (28.8 dBm) has been achieved with 5 dB gain.

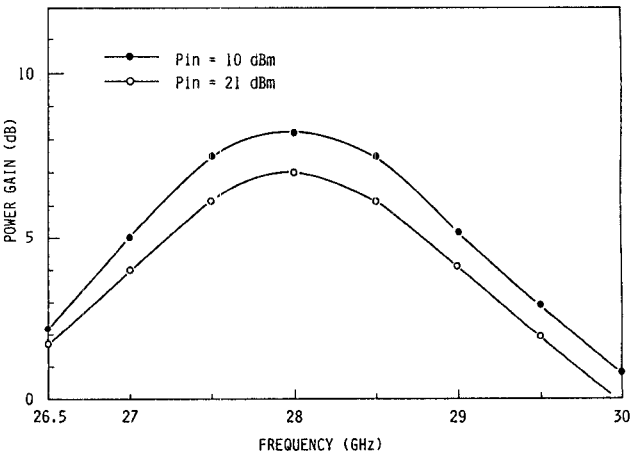

Fig.7. Typical frequency response for two-stage amplifier

CONCLUSION

A Ka-band monolithic GaAa two-stage amplifier with large gate width has been developed. The amplifier delivers an output power of 0.56 W at 1dB gain compression point with 7.2 dB gain and 15 % power-added efficiency. Further improvements in output power can be achieved through drain currents optimization and a monolithic parallel combining of amplifiers.

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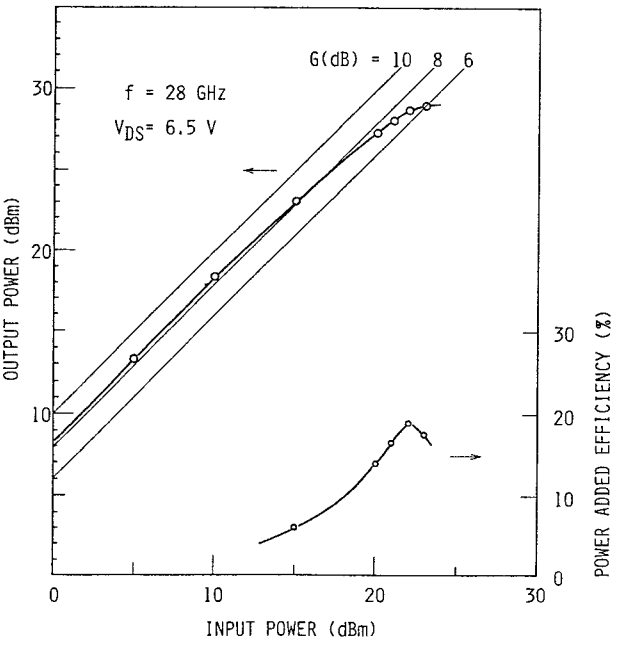

Fig.8. Typical input-output characteristics for two-stage amplifier